Claims 1 and 3 have been amended; and no claims have been newly added. Applicants respectfully submit that no new matter has been added by this amendment.

In the outstanding Office Action, Claims 1 and 8-10 were rejected under 35 U.S.C. § 102(b) as anticipated by Matsumura et al. (JP 58-124243, hereafter "JP '243"); Claims 1 and 8-10 were rejected under 35 U.S.C. § 102(e) as anticipated by Kunikiyo (U.S. Pat. No. 6,429,505); Claims 1-3, 8, and 9 were rejected under 35 U.S.C. § 102(a) as anticipated by Maeda et al. (EP 1 115 158, hereafter "EP '158"); Claims 1 and 8-12 were rejected under 35 U.S.C. § 102(a) as anticipated by Matsumoto et al. (JP 2001284599, hereafter "JP '599"); Claim 11 was rejected under 35 U.S.C. § 103(a) as unpatentable over JP '243 in view of Higashi et al. (EP 962988, hereafter "EP '988"); and Claim 12 was rejected under 35 U.S.C. § 103(a) as unpatentable over JP '243 in view of EP '988 as applied to Claims 1 and 11 and further in view of Redwine et al. (U.S. Pat. No. 5,349,225, hereafter "the '225 patent").

Applicants thank Examiner Sefer and Supervisory Examiner Flynn for the interview granted Applicants' representatives on October 23, 2002. During the interview, proposed amendments to Claim 1 were discussed with regard to JP '243. No exhibits were shown, and no demonstrations were conducted. While no agreement was reached as to the allowability of any claims, Applicants' representatives and the Examiners were better able to understand each others' positions.

With regard to the rejection of Claims 1 and 8-10 under 35 U.S.C. § 102(b) as anticipated by JP '243, Applicants respectfully submit that this rejection has been overcome by the present amendment. Because Claim 1 recites features previously recited in Claim 2, it is respectfully requested that this rejection be withdrawn.

With regard to the rejection of Claims 1 and 8-10 under 35 U.S.C. § 102(e) as anticipated by Kunikiyo, this rejection is respectfully traversed. Claim 1 has been amended

to incorporate the limitations of Claim 2. Accordingly, it is respectfully submitted that this rejection is overcome.

With regard to the rejection of Claims 1-3, 8 and 9 under 35 U.S.C. § 102(a) as anticipated by EP '158, this rejection is respectfully traversed. Claim 1 as amended is characterized in that the body region potential setting section includes a body region source/drain adjacent portion in a gate width direction adjacently to the source and drain regions and extended in a gate length direction from the body region main part. The gate electrode further has the gate extension region extended in the gate length direction from an end of the gate electrode main part and formed on a part of the body region source/drain adjacent portion, and serving to electrically block the body region source/drain adjacent portion and the source and drain regions through the gate extension region.

In the outstanding Office Action, it is indicated that the under semiconductor layer 10c in Figs. 7 and 8 of EP '158 corresponds to the body region source/drain adjacent portion of the present invention. However, the under semiconductor layer 10c of EP '158 is formed under the gate electrode 15 between the source and the drain 11, and corresponds to the channel region of the transistor. It should be noted that Fig. 8 shows the broken off and bent 8-8 section of Fig. 7.

More specifically, just as with the ordinary channel region, the under semiconductor layer 10c of EP '158 is adjacent to the source and the drain regions in a gate length direction and extends in a gate width direction. Thus, it can be said that this structure is completely distinct from the body region source/drain adjacent portion according to the present invention.

In addition, although the Office Action indicates that the sidewall 15b of EP '158 corresponds to the gate extension region of the present invention, it is obvious that the

sidewall 15b is an insulator and consequently it does not function as a gate electrode. Furthermore, given that the gate electrode 15e on the under semiconductor layer 10c corresponds to the gate extension region of the present invention, it becomes obvious that the gate electrode 15e on the under semiconductor layer 10c of EP '158 differs from the gate extension region of the present invention. Specifically, the under semiconductor layer 10c described in EP '158 is distinct from the body region source/drain adjacent portion according to the present invention (which is formed on a part of the body region source/drain adjacent portion) for the reasons mentioned above. Therefore, both of the sidewall 15b and the gate electrode 15e on the under semiconductor layer 10c are distinct from the gate extension region of the present invention.

As discussed above, EP '158 does not disclose or even suggest the body region source/drain adjacent portion and the gate extension region according to the present invention.

Furthermore, in Claim 1 as amended, the thickness of the partial insulating film lower semiconductor region is thinner than that of the source and drain regions, thereby enabling the existence of finite resistance in the partial insulating film lower semiconductor region. Therefore, the semiconductor device recited in Claim 1 as amended has an effect of fixing the body potential in a stable manner, since the gate electrode has the gate extension region.

Consequently, it is respectfully submitted that independent Claim 1 patentably distinguishes over EP '158. Likewise, since each of Claims 3 and 8-10 depends from Claim 1, it is respectfully submitted that these claims patentably distinguish over EP '158.

In response to the rejection of Claims 1 and 8-12 under 35 U.S.C. § 102(a) as anticipated by JP '599, Applicants, as earlier noted, have submitted concurrently herewith a certified English translation of the priority document. The publication date of JP '599 is

October 12, 2001, subsequent to the Applicants' perfected priority date. Accordingly, JP '599 is not available against the present claims under 35 U.S.C. § 102(a). Applicants therefore respectfully request that this rejection be withdrawn.

In response to the rejection of Claim 11 under 35 U.S.C. § 103(a) as unpatentable over JP '243 in view of EP '988, Applicants respectfully submit that the Office Action has failed to provide a *prima facie* case of obviousness. Claim 11 depends from amended Claim 1.

At the outset, Applicants respectfully submit that there is no motivation in either of the teachings of these references in support of the proposed combination. As stated in MPEP § 706.02(j), "[t]o establish a *prima facie* case of obviousness ... there must be some suggestion or motivation ... to modify the reference or to combine reference teachings ...." Applicants respectfully submit that this requirement of a *prima facie* case has not been satisfied.

JP '243 relates to a semiconductor device configured to eliminate the floating state of the substrate.[2] As noted above, JP '243 fails to disclose or suggest the limitations recited in independent Claim 1. Additionally, as admitted in the Office Action at page 9, JP '243 fails to disclose or suggest a depletion layer extended from said drain region that reaches the buried insulating layer during normal operation.

EP '988 relates to a semiconductor device in which driving capability in an active state is improved and electric current consumption in a standby state is reduced.[3] Unlike the present invention and JP '243, however, EP '988 is not directed toward elimination of a floating-body effect. In fact, there is no suggestion in the disclosure of EP '988 that the

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[2] JP '243, Abstract.

[3] EP '988, col. 1, lines 10-12.

configuration disclosed therein would be in any way useful for eliminating the floating state of the substrate in a semiconductor device. Accordingly, Applicants respectfully submit that one of ordinary skill in the art would not have been motivated to modify JP '243 in the manner suggested by the Office Action.

Moreover, the Office Action fails to cite to any specific teachings in either of the references to support the proposed combination. Applicants therefore respectfully submit that the proposed combination is based solely upon hindsight, and request that this rejection be withdrawn.

With regard to the rejection of Claim 12 under 35 U.S.C. § 103(a) as unpatentable over JP '243 in view of EP '988 and further in view of the '225 patent, Applicants respectfully submit that the Office Action has failed to provide a *prima facie* case of obviousness. Claim 12 depends from Claim 1.

As noted above, Applicants respectfully submit that the combination of JP '243 and EP '988 is based solely upon hindsight. Applicants respectfully submit that the addition of the '225 patent to this combination represents additional hindsight reconstruction. As further noted above, the combination of JP '243 and EP '988 fails to disclose the Applicants' claimed limitations.

The '225 patent relates a field effect transistor with a lightly doped drain. However, in no way does the '225 patent address eliminating the floating state of the substrate. The '225 patent certainly fails to disclose or suggest that the configuration disclosed therein would be useful for eliminating the floating state of the substrate. Since the structure described in Redwine is a transistor structure formed on a bulk substrate, it is impossible to anticipate the structure of the semiconductor device recited in Claim 12, which is intended to suppress the floating-body effect produced in a transistor formed with an SOI structure.

Accordingly, as there is no suggestion in the teachings of the '225 patent in support of the proposed combination, and the Office Action fails to cite to any specific teachings any of the references in support of the proposed combination, Applicants respectfully submit that the proposed combination is based solely upon hindsight. Applicants therefore respectfully request that this rejection be withdrawn.

Consequently, in view of the foregoing discussion and present amendments, Applicants respectfully submit that the pending application is in condition for immediate allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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IN THE SPECIFICATION

Please amend the specification at page 1, line 19 through page 2, line 7 as shown below:

The complete isolation technique is characterized by being latch up free (latch - up is not caused), [a resistance to noises] and resistant to noise and the like because the element is electrically isolated completely from other elements. However, since a transistor is operated in an electrical floating state, there is a problem in that a frequency dependency is caused on a delay time and a floating-body effect, for example, a kink effect in which a hump is generated on a drain current - drain voltage characteristic or the like [is produced]. In order to suppress the floating-body effect, an isolation oxide film (partial oxide film) is formed in an upper layer portion so as not to come in contact with the buried oxide film and constitutes a partial isolation region together with a part of an SOI layer in a lower layer portion and a body terminal is provided in a body region formed in a region isolated in the partial isolation region. Consequently, a partial isolation technique capable of fixing [s] a substrate potential (body potential) through the SOI layer provided under the partial oxide film is effective. However, there is a problem in that the partial isolation technique does not have the latch up free which is the advantage of the complete isolation technique.

Please amend the specification at page 18, line 22 through page 19, line 1 as shown

below:

Moreover, a body region 10 (a body region outside an element formation region) is isolated by the partial oxide film 31 [an] and the p well region 11 provided thereunder and is formed from the surface of the SOI layer 4 to the back face thereof. The body region 10 is electrically connected to a main part of the body region to be the SOI layer 4 provided under the gate electrode 7 through the p well region 11.

IN THE CLAIMS

--1. (Amended) A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulating layer and an SOI layer, comprising:

a MOS transistor provided in an element formation region of said SOI layer; and

a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region to be a part of said SOI layer present in a lower layer portion of said SOI layer,

said MOS transistor including:

source and drain regions of a first conductivity type selectively formed in said SOI layer, respectively;

a gate electrode having a gate electrode main part formed through a gate oxide film on a region of said SOI layer between said source and drain regions; and

a body region having a body region main part to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion electrically connected from said body region main part

in said element formation region and capable of externally fixing an electric potential,

wherein said body region potential setting section includes a body region source/drain adjacent portion in a gate width direction adjacently to said source and drain regions and extended in a gate length direction from said body region main part,

said gate electrode further includes a gate extension region extended in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, and serving to electrically block said body region source/drain adjacent portion and said source and drain regions through said gate extension region, and

a thickness of said partial insulating film lower semiconductor region is thinner than a thickness of said source and drain regions.

2. (Cancelled)

3. (Amended) The semiconductor device according to claim [2] 1, wherein

said body region source/drain adjacent portion includes a first body region source/drain adjacent portion extended in a first direction from said body region main part and a second body region source/drain adjacent portion extended in a second direction opposite to said first direction from said body region main part, and

said gate extension region includes a first gate extension region formed on a vicinity of said first body region source/drain adjacent portion and a second gate extension region extended on a vicinity of said second body region source/drain adjacent portion.

4. (Amended) The semiconductor device according to claim [2] 1, wherein

said body region source/drain adjacent portion includes one body region source/drain adjacent portion, and

said gate extension region includes one gate extension region formed on a vicinity of

said body region source/drain adjacent portion.

5. (Amended) The semiconductor device according to claim [2] 1, wherein said body region source/drain adjacent portion has a high concentration region having a higher impurity concentration of a second conductivity type than that in other regions over a region provided apart from said gate extension region by a predetermined distance.

6. (Amended) The semiconductor device according to claim [2] 1, wherein said gate extension region includes a gate extension region having an impurity concentration of the second conductivity type of 5×10^{18} cm^{-3} or less.--